

FPGA-based Real-Time Hardware-In-the-Loop Simulator of a Mini Solar Power Station

T. Debrececi ¹, T. Kökényesi ^{#2}, Z. Sütő ^{#3} and I. Varjasi ^{#4}

[#] *Department of Automation and Applied Informatics, Budapest University of Technology and Economics
Magyar tudósok krt. 2. (Bldg. Q.), Budapest H-1117, Hungary*

² *tamas.kokenyesi@aut.bme.hu*

³ *zoltan.suto@aut.bme.hu*

⁴ *istvan.varjasi@aut.bme.hu*

^{*} *Siemens Zrt.*

Gizella út 51-57., Budapest H-1143, Hungary

¹ *tibor.debrececi.ext@siemens.com*

Abstract—Nowadays as the technology is developing, the more complex the power electronics and its controls become, the more proper hardware tool is required for HIL (Hardware-In-the-Loop) simulation. The general aim of the presented work is developing a fast, reliable and scalable HIL simulation framework for the rapid prototyping of complex power electronic systems. There are at least three strong reasons for using HIL simulation during the development: i) reduction of development time, ii) safety and quality requirements, and iii) prevent costly and dangerous failures [1].

The subject of the paper is the development of such a real-time HIL simulator using an FPGA. The system to be modeled is a mini solar power station with energy storage, which means that it is a solar panels-fed battery charger power stage with the battery itself.

Index Terms—HIL Simulation, FPGA, Rapid Prototyping, Power Electronics, Real-Time Simulation, Solar Panels, Renewable Energy.

I. INTRODUCTION

The development of the control unit for modern power converters is nowadays a very cost- and time-critical task. In contrast to this, quick answers are expected for the claims by the market, certainly without quality loss.

A general power converter consists of two main parts: a power level (main circuit) and a digital controller unit, which is usually realized by using some kind of DSP. Remarkably complex and multiple controls are required for the state-of-the-art power conversion tasks, and the field test (test on the real main circuit) of these control units can be dangerous not just for the system itself, but for the testers. A low-power model of the main circuit can be built under laboratory conditions, but it will have parameters differing from the ones of the original system. Generally it is not possible to set the same time constants as in the real system, and the relative losses are also higher [1].

The main concept of using HIL (Hardware-In-the-Loop) simulation in power electronic systems is that computational models replace the high-power parts of the system. The simulated parts are connected through real physical interfaces like analog and digital channels to the control boards under development, so the boards can be tested and validated in their

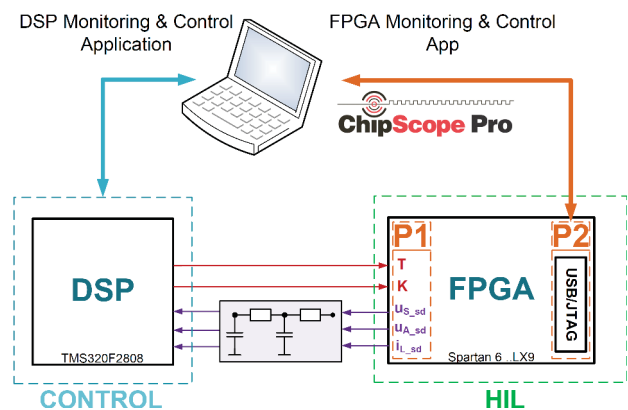


Figure 1. The main block diagram of the HIL simulator based test environment of the DSP controller.

seemingly real environment [2]. The HIL simulator is now the model of the power converter with its supply and its load implemented on an FPGA [3], [4], [5]. The HIL simulation is a very useful and practical tool in the power electronics, the simulator can be parameterized, monitored, it works on logic level, thus the test of a newly designed control unit can be done quickly and without any danger. The extreme failure cases are also reproducible, which would happen very rarely in the real system.

The further benefit of this test method in contrast to the computer-based simulation method is that it can be attainable to have the same signal levels of the IOs of the control unit board as the signal levels of the interface (control and measured signals) between the control and the main circuit, thus the hardware- and the software test of the control electronics can be fulfilled.

In the development of the HIL simulator we have to try to get a proper ratio of the cost/quality, and for that the FPGA-implementable model of the main circuit can be defined on high level program language (Matlab/Simulink and HDL Coder), so that less work remains with the code optimization

during the development.

II. SYSTEM SETUP

The system consists of an FPGA-based HIL simulator and of a DSP-based Control Unit (CU), it can be seen on Fig. 1. Human Machine Interfaces (HMIs) were designed to help the testing process. Both units are connected to a computer, on which Graphical User Interfaces ensure the possibility to set and monitor signals according to the user's claims.

III. THE MODELED SYSTEM

The modeled system is a solar-based battery charger. The schematic diagram of the main circuit can be seen in Fig. 2. The circuit is controlled by two logical input signals, the PWM signal T controls the IGBT and the signal K controls the DC contactor. The DSP controller measures three analog signals, the inductor current i_L , the voltage of the solar panel u_S and the battery voltage u_A , and based on these values and the charging current reference the controller fulfills the control actions.

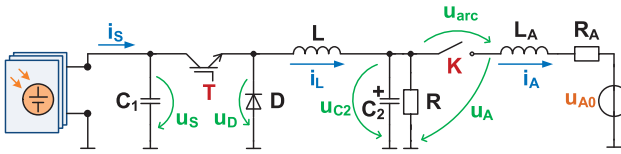


Figure 2. Main circuit of the solar charger modeled in the HIL.

The parameters of the solar panels can be modified from the HMI of the simulator. In the developed simulator it is possible to emulate the operation of 3 solar panels together, naturally there can be more panels, but 3 pieces are enough to demonstrate the method. The 3 solar panels are in parallel connection, their Open Circuit (OC) voltages and Short Circuit (SC) currents can be set at run-time, and thus the given normalized characteristics can be scaled by the user during operation. To make the real-time calculations faster, divisions should be avoided in the FPGA, so the inverse of the OC voltages are given by the user. There are also output signals for monitoring in the HMI. All the interface signals of the HIL simulator can be seen in Table I.

A. Solar Panels

The current-voltage characteristics of an existing solar panel (MSX-60) was taken as a basis for the model creation [6].

Table I
INTERFACING OF THE HIL SIMULATOR

Type	Notation	Details
Parameters	$U_{ocA}^{-1}, U_{ocB}^{-1}, U_{ocC}^{-1}, I_{scA}, I_{scB}, I_{scC}, U_{A0}$	Command from the HIL HMI
Control signals	T, K	From the CU (DSP board)
Outputs	u_S, u_A, i_L	To the CU (DSP board)
Monitoring	$u_S, i_S, u_D, i_L, u_{C2}, u_A, i_A$	Function in the HIL HMI

The normalization of this characteristics was done by division of voltage values with the open circuit (OC) voltage and by division of current values with the short circuit (SC) current value. On Fig. 3 normalized characteristics can be seen.

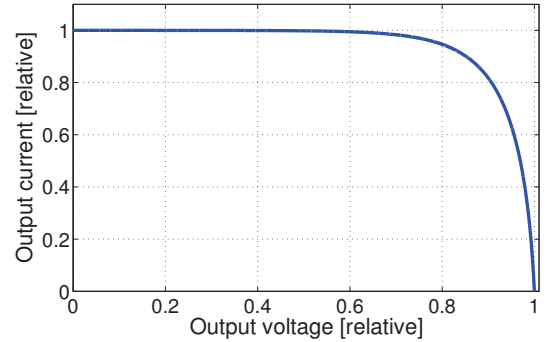


Figure 3. Normalized solar panel characteristics.

It can be said with a first approximation, that the temperature parameter affects particularly the OC voltage; the radiation parameter affects particularly the SC current of the characteristics. The increase of the temperature leads to the decrease of the OC voltage and the increase of the radiation leads to the increase of the SC current on the characteristics. Therefore the user can analyze the effects of these parameters on the system.

The summation characteristics of the solar panels turn out as follows: the voltage of the load of the solar PV system and the OC voltage parameters define the positions on the voltage axis of the three normalized characteristics. On the basis of this three current values turn out, these should be multiplied by the SC current values set by the user. The three current results are added together to have the final output current value of the solar PV system, which can be seen on Fig. 4.

B. The Battery Charger Unit

The next part with the IGBT, diode D , inductance L and the capacitor C_2 with the parallel discharging resistor R represents an asynchronous step-down (buck) converter; the voltage of the capacitor C_2 has to be held by control of the current i_L . After pre-charging, the connected battery to the output can be switched to the converter by the DC contactor.

The IGBT and the DC contactor are switched on when their digital control signals (in order T and K) are in logical high state, otherwise they are switched off. All components are assumed as ideal items except the DC contactor as described below.

C. The Battery

The model of the battery consists of a voltage source u_{A0} , a series resistance R_A and inductance L_A , which are representing the inner impedance.

D. Functional Description

The main circuit model was made by using state-space modeling [5], [7]. The current i_S turns out based on value u_S

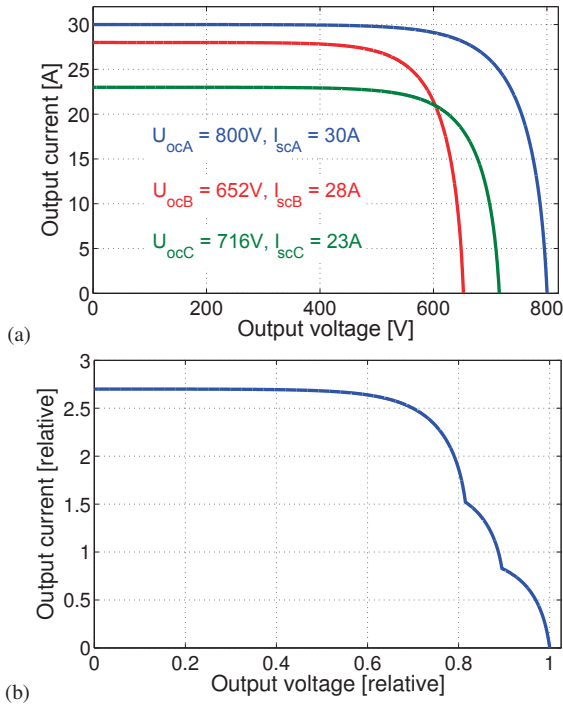


Figure 4. (a) Example characteristics for three solar panels and (b) the summed normalized characteristics. The normalization was done to $U_{oc} = 800$ V and $I_{sc} = 30$ A.

from the summation characteristics of the solar PV system, which charges the capacitor C_1 . The next stage is the step-down converter, hereby the current i_L of coil L , and indirectly the pre-charge of capacitor C_2 are controlled. $i_L \geq 0$, since the diode D is ideal, so reverse current cannot flow on it, nor on the IGBT to the capacitor C_1 .

After pre-charging, the battery is switched onto the charger. While the DC contactor is conducting, the battery voltage u_A is u_{C2} , but in the case of switching off and the current is still flowing, the arc voltage U_{arc} of the DC contactor has to be handled. When the current reaches zero, the contactor becomes opened and the voltage u_A equals to u_{A0} .

According to the description above, the integral equations of the dynamic operation are the followings:

$$u_S = \frac{1}{C_1} \int_0^t (i_S - T i_L) dt \quad (1)$$

$$i_L = \frac{1}{L} \int_0^t (u_D - u_{C2}) dt, \text{ where } i_L \geq 0 \quad (2)$$

$$u_{C2} = \frac{1}{C_2} \int_0^t \left(i_L - i_A - \frac{u_{C2}}{R} \right) dt \quad (3)$$

$$i_A = \frac{1}{L_A} \int_0^t (u_A - U_{A0} - R_A i_A) dt \quad (4)$$

where the diode voltage u_D can be expressed by the following piece-wise defined equation:

$$u_D = \begin{cases} u_S & \text{if } T = 1 \\ 0 & \text{if } T = 0 \text{ and } i_L > 0 \\ u_{C2} & \text{if } T = 0 \text{ and } i_L = 0 \end{cases} \quad (5)$$

Here we have assumed ideal switching behaviors for both the diode and the IGBT. Due to the DC contactor model with the arc voltage U_{arc} , the accumulator voltage u_A can be written as

$$u_A = \begin{cases} u_{C2} & \text{if } K = 1 \\ u_{C2} - U_{arc} & \text{if } K = 0 \text{ and } i_A > 0 \\ U_{A0} & \text{if } K = 0 \text{ and } i_A = 0 \end{cases} \quad (6)$$

IV. THE SIMULINK MODEL

The entire model can be seen on Fig. 5. It is divided into two main blocks: the first is the system of the three solar panels connected in parallel (Solar Panels). The current output i_S is connected to the next stage (Main Circuit), which contains the model of the battery charger and the battery. The Main Circuit block determines the solar voltage u_S which is connected as an input to the Solar Panels block.

The Simulink model has got nine inputs and ten outputs. Two out of the input signals are connected to the Main Circuit block. The digital control signal T of the IGBT and the digital control signal K of the DC contactor arrive from the DSP CU. The other seven inputs are adjustable parameters of the system, the OC voltage and SC current parameters of the solar panels and the OC battery voltage U_{A0} used by the Main Circuit block.

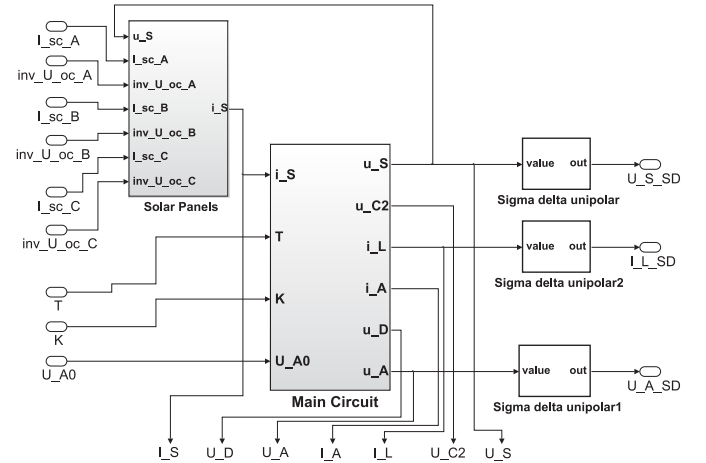


Figure 5. Subsystem of the HIL simulator.

Seven output signals are inner signals monitored by the HMI of the FPGA and three signals are connected to the output pins of the FPGA for the CU. The DSP CU expects analog signals u_S , u_A and i_L from the HIL. However analog signals directly cannot be outputted by the FPGA, sigma-delta D/A converters were used.

A. Sigma-Delta Modulators

This D/A converter type is very similar to a PWM generator: the generated duty cycle at the output will be proportional to the input value. In order to reach the proportional analog

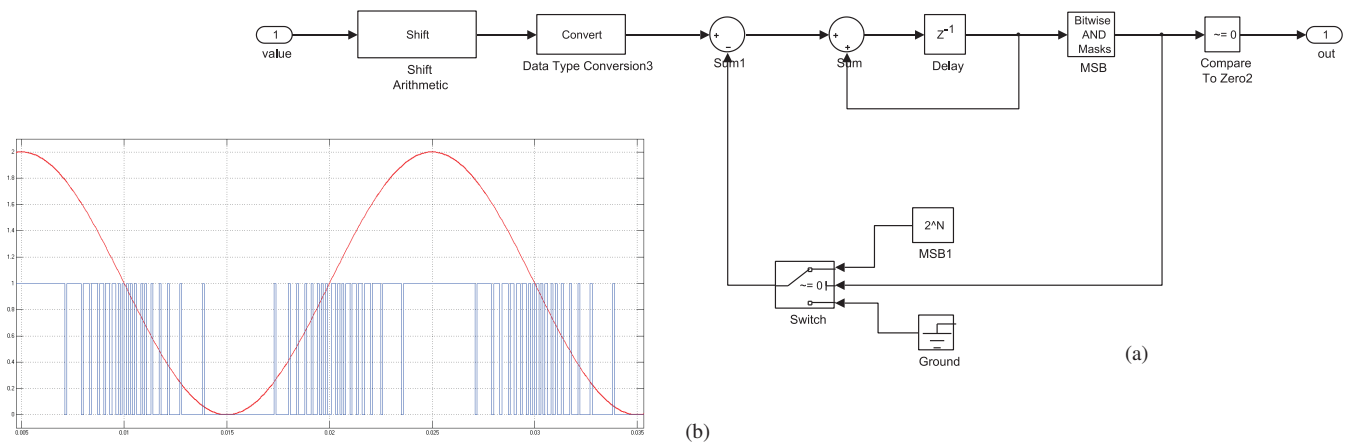


Figure 6. (a) Sigma-delta D/A converter. (b) Example for sigma-delta D/A conversion.

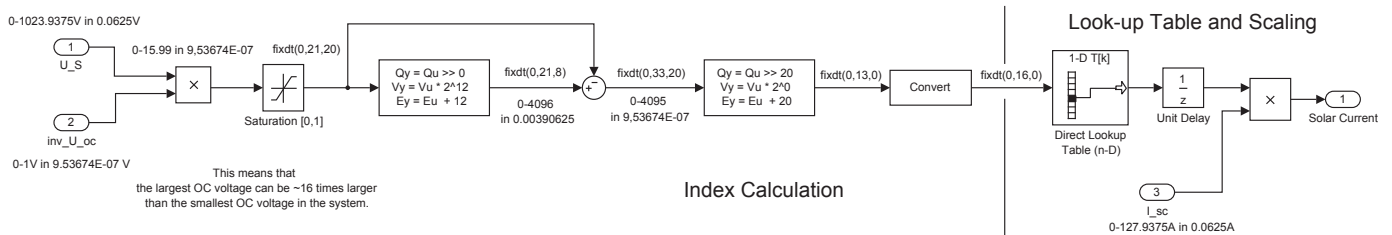


Figure 7. Simulink model of the look-up table based solar panel.

value, analog filters (RC circuits) are required to connect the corresponding FPGA pins to the A/D channels of the DSP controller (Fig. 1). Note that, filters with higher cut-off frequency can be applied for sigma-delta signals than for PWM signals, so sigma-delta D/A converters are able to generate faster analog signals.

The detailed operation is the following: The signal to be modulated comes to a first order integrator [8]. If it overflows, the value of the output pin is 1 and then the maximum value is subtracted from the integrator. Otherwise the output is 0 and nothing else happens. In the Simulink model, it was done by bit masking and data type conversions between the different wide fixed-point representations [see Fig. 6(a)]. The output waveform will be a series of short impulses with the length of one clock cycle. The more the converted value is, the more frequent are the impulses, therefore the duty cycle also rises. An example signal (a sine waveform) and its sigma-delta modulated output can be seen on Fig. 6(b).

B. The Solar PV System

The current-voltage characteristics of the MSX-60 type solar panel ([6]) has been implemented in a Matlab *m*-file. This curve was normalized to 1 and its relative voltage was divided to 4096 discrete values. Thus there is a vector with 4096 elements, which can be addressed with 12 bits. The indexes of the vector run from 0 to 4095 in a resolution of 1, and the values belonging to the indexes are the relative current values from the normalized characteristics.

For the hardware implementation, the storage of the vector and an indexer unit are needed. As the relative current value has turned out from the stored characteristics, just a multiplication is required by the SC current value to have the final output current value of a solar panel (see Fig. 7 right side).

The user can set the inverse of value U_{oc} , so the division function can be avoided. Then the index turns out correctly. To save FPGA hardware resources (especially multipliers), the multiplication with 4095 can be replaced with a subtracting from its 12 bit left shifted value and some additional conversion for fixed point representation. The model of this index calculation can be seen on Fig. 7.

This index is used to get the position on the voltage axis of the normalized characteristics. The result can be larger than 1. It is because of the OC voltages of the three solar panels can be different, so the value of u_S can be larger than the lowest two OC voltages among the different panels. In this case $u_S > U_{oc}$ can be obtained, and thus the final index should be saturated between 0 and 4095. It results in zero output currents in the solar panels with the lower OC voltages.

The index has to address the vector, which stores the normalized characteristics for each panels. The final output current i_S of the solar PV system turns out as the summation of the three currents.

In the Simulink model, a one dimension look-up table and a one cycle delay is needed for this functionality. After code generation, the HDL synthesis tool can recognize this construction (see Fig. 7 right side) and create the look-up

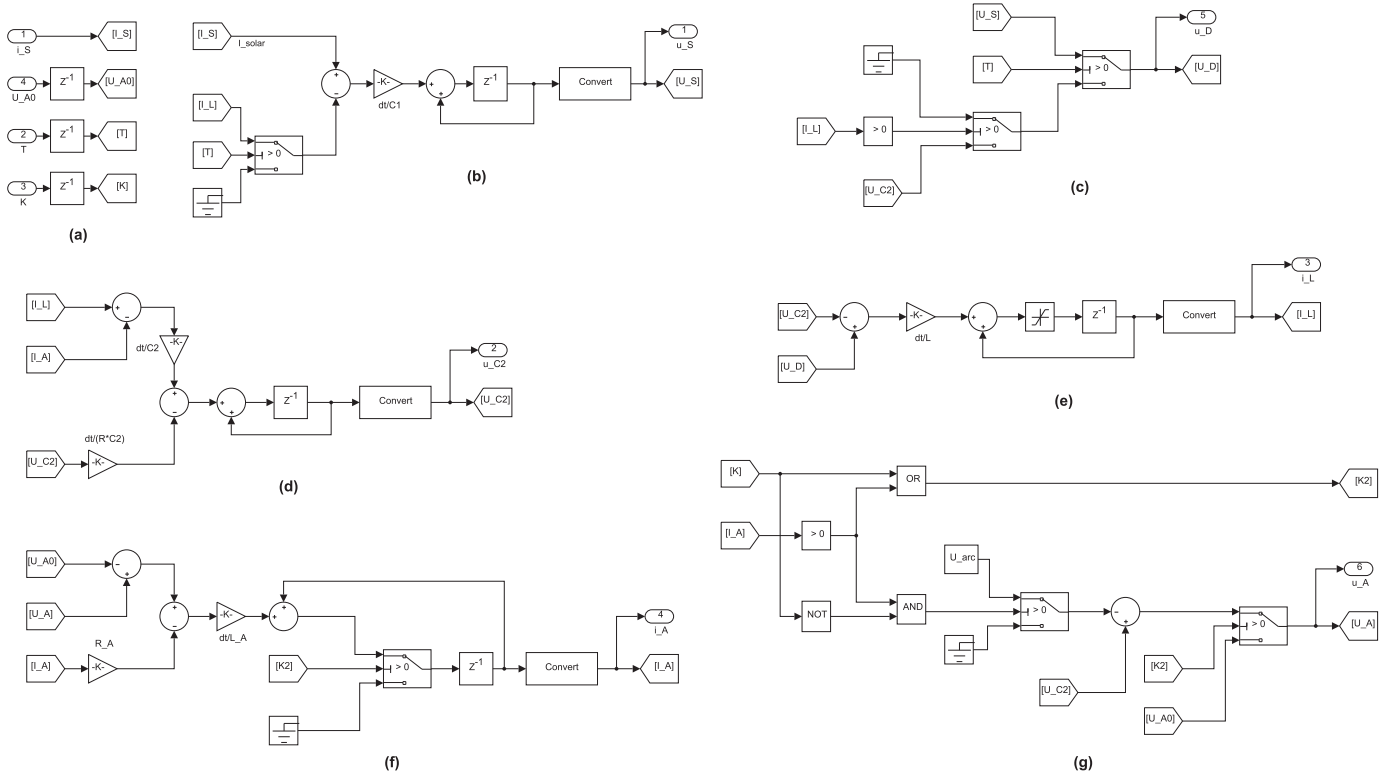


Figure 8. (a) Initial zero-order hold of the input signals. HDL capable implementations of the integral equations of (b) the solar voltage u_S , (c) the diode voltage u_D , (d) the inductor current i_L , (e) the output voltage of the buck-converter u_{C2} and (f) the accumulator current i_A and the relating equation (g) with the contactor arc voltage U_{arc} [see eq. (1)–(6)].

tables from block RAMs in the FPGA.

C. Main Circuit Model

The dynamic model of the solar charger expressed by eq. (1)–(6) has been built up inside the Main Circuit Simulink block. The inner structure of this block can be seen in Fig. 8. The model has to consist of only synthesizable elements, especially adder, subtractor, multiplier, delay, holder, conditional expression (switch) and general logical elements. The model was designed with fixed-point data formats. The inner values, e.g. the accumulator values of the discrete-time integrators are important to be handled in the system without data losses. There are Fixed-point tools in Simulink which supports the automatic selection of a fixed-point representation in the knowledge of the minimum and maximum values of the signals and the required precisions, but in this system the proper fixed-point representations for the signals have been set manually.

D. HMI

In the case of the DSP-based CU, designing the HMI is a common task, but in the case of the FPGA-based HIL, this is not such an obvious task to do. The Xilinx's ChipScope Pro is a utility tool for viewing and/or modifying inner signals in the FPGA at run-time. By means of this utility a HMI for our design can be created, for example to set the parameters for the solar panels (OC voltages and SC currents) or the state

of charge of the accumulator by its no-load voltage U_{A0} . An empty subsystem block can be placed in the model in Fig. 5 to define the ChipScope interface using the inner input and output signals of the adjustable/viewable parameters. Setting the HDL architecture property of this subsystem block to BlackBox, it allows to implement the block by self-written HDL code. By means of this option the ICON, VIO and/or ILA cores of ChipScope Pro can be easily included and the proper connections can be realized between them to create the HMI for the FPGA simulator.

V. TEST RESULTS

The measurements have been done by the designed ChipScope Pro based HMI of the FPGA used IP cores. The highest voltage of the solar panels is 600 V, summation of the SC currents is 50 A, while the open circuit battery voltage U_{A0} is 400 V.

The DSP and FPGA boards were connected on a Digilent intelligent breadboard, with a built-in oscilloscope function. It is possible to display the signals as shown on Fig. 9 during the start-up process. At the pre-charge period, current i_L is controlled and the voltage u_{C2} is estimated by the controller. While there is no current i_A flowing in the battery, the voltage of the battery equals to the value U_{A0} . When the estimated value is larger than the voltage of the battery, the CU turns on the DC contactor. At this time, capacitor C_2 is switched onto the battery, as it can be seen on Fig. 9. After the pre-charge,

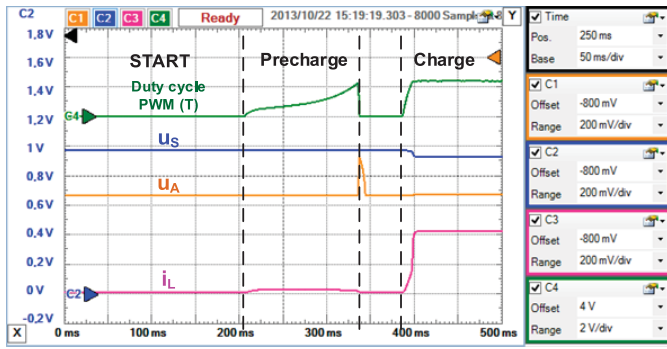


Figure 9. Startup process.

there is a voltage spike in the signal u_A , which shows the switching event.

The contactor switches right after the control signal K rises, since the mechanical delay of the contactor is not taken into account. After that, the charging begins. Because of the low value of the pre-charging current, the value u_S of the solar PV supply decreases marginally, but at the charge period it is significant. On the summation characteristics of the solar PV system the higher current values belong to the lower voltage values, that current is needed to complete the charging.

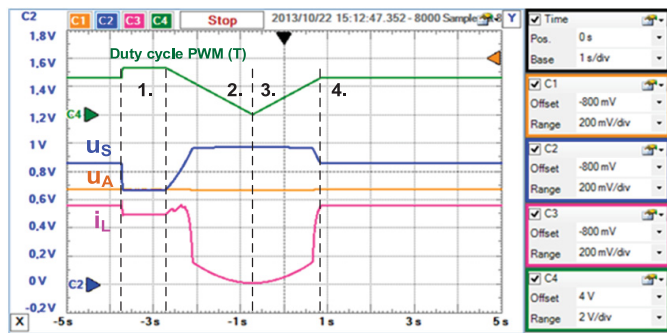


Figure 10. MPPT operation.

On Fig. 10 the process of the Maximum Power Point Tracking (MPPT) algorithm can be seen. Much larger current reference is given to the current controller than the solar PV supply can ensure in power. If the load expects larger power than the solar PV supply can ensure the duty cycle is saturated at unit value (stage 1), then the operation on the MPP is the best solution.

The CU steps down the duty cycle of the PWM signal T from 100 % to 0 % with given steps, and saves the measured power values (stage 2). To avoid the current spikes due to the leap of the duty cycle value, the duty cycle is set through a safe gradient, which the largest power value belongs to (stage 3). Until the current reference or the insolation level of the solar panels does not change, the CU holds on the value of the duty cycle (stage 4).

VI. CONCLUSION

The paper introduced the development of the HIL simulator for a power system, which consists of a solar PV supply, and an energy storage by charging a storage battery. The affects of the temperature and radiation of the solar panels can be indirectly set by the user/developer in real-time by scaling normalized characteristics stored in block RAMs. We have been trying to get a proper ratio of the cost/quality, and for that the FPGA-implementable model of the main circuit was defined in Matlab/Simulink, so that less work remained with the code optimization during the development, and a deep knowledge about the FPGA development environment (Xilinx ISE) is not needed. The development process from creating the models to generating the implementation files, building the binary code for programming the device and either the programming itself can be done from a unified environment in Matlab.

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